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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,257	10/03/2003	Satoshi Inoue	039282.03	9107

25944 7590 11/28/2005

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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
10/677,257			

EXAMINER	
ART UNIT	PAPER
	20051120

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Commissioner for Patents

*** ATTACHMENT IS A CORRECTED PAGE 5 OF THE LAST OFFICE ACTION MAILED NOVEMBER 02, 2005.

*** IN RESPONSE TO APPLICANT'S REQUEST IN REMARKS FILED AUGUST 15, 2005, A PTO-892 FORM CITING YAMAZAKI (5,514,879) IS INCLUDED.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Michael Trinh
Primary Examiner

10/677,257

opposites sides of the second region, the first end of the second region being in a side opposite the plurality of third regions 17 (Figs 2,1).

Claim Rejections - 35 USC § 103

1. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over either Nakagawa et al (5,477,065) or Okada (5,294,824, taken with Kawashima et al (5,016,986).

Nakagawa teaches a method for forming a transistor as applied to claims 8,9,22,30 above. Okada also teaches a method for forming a transistor as applied to claim 8 above.

Re claims 17-20, Nakagawa or Okada already teaches the method of manufacturing the transistor, but lacks using the method for manufacturing an active matrix substrate (claim 17), an electroluminescent device (claim 18), display device (claim 19), and an electronic apparatus (claim 20).

However, Kawashima teaches (at col 10, lines 60-68) applying the method in manufacturing a liquid crystal display as active matrix substrate (claim 17) and other devices including a plasma display device (re claim 19), an electroluminescence display device (claim 18), and electronic devices (claim 20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the method of manufacturing the transistor of Nakagawa or Okada in manufacturing other devices including the active matrix substrate as liquid crystal display, the electroluminescence display device, the plasma display device, and the electronic devices, as taught by Kawashima. This is because of the desirability to manufacture different and various types of devices by using transistors having high speed operation with lower power consumption.

2. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over either Nakagawa et al (5,477,065) or Okada (5,294,824), taken with Yamazaki.

Nakagawa teaches a method for forming a transistor as applied to claims 8,9,22,30 above. Okada also teaches a method for forming a transistor as applied to claim 8 above.

Re claim 15, Nakagawa or Okada already teaches forming a semiconductor film, but lacks applying an energy to crystallize the semiconductor film before forming the second region.